REMARKS

Entry of this Amendment is proper under 37 CFR §1.116, since there are no new issues raised herein that necessitate a new search and the only substantive claim amendments are attempting to find wording acceptable to the Examiner.

Applicants gratefully acknowledge Examiner Vicary for courtesies extended during a telephone interview dated May 13, 2009, including co-inventor Dr. Gustavson.

During this interview, Applicants explained how they considered that the latest Office Action could be distilled to three primary concerns, all related to specific claim wording and adequate support in the specification for the current version of the claim wording. More specifically, Dr. Gustavson explained that he considered that the claims should be allowable over his previous word, the only cited prior art reference currently of record, if Applicants addressed the claim wording "scheduling", "reducing", and "small".

Examiner Vicary indicated that he agreed that these three words should be addressed in a manner suggested in the latest Office Action, but also expressed concern that the text added to the specification in support of revised claim wording be worded consistent with the language from co-pending applications rather than rephrased in different terms, even if Applicants did consider that one of ordinary skill in the art would better understand the alternate terminology.

Applicants then described how the expression "k > 1", relative to describing SIMD (single instruction, multiple data) in the claim language, is intended to indicate the number of data words involved in the single instruction, not that there are a plurality of SIMD units, as the rejection suggests. For example, co-pending application, US Patent Application S/N 10/671,888, describes the register block format involves using the quad format, wherein the four data words in a "pseudo matrix" block (which is used in that application to explain the more generic concept of the register block format) were transferred using a single instruction, including the capability to crisscross the data words to overcome an interface concern at the FPU. Thus, Applicants explained how this example demonstrates "k > 1" in this co-pending application, in the manner intended in the claim language of the present application.

Applicants again pointed out that machines with SIMD (k > 1) capability were not available at the time of the publication of the reference cited against the claimed invention, so that the concepts described in the independent claims would not be demonstrated by this publication. Dr. Gustavson also pointed out that the value of *k* depends upon whether the

instruction involved, for example, single precision versus double precision.

Finally, Applicants again pointed out that the cited reference, one of Dr. Gustavson's own previous publications, differed from the claimed invention, since it required 12 streams of data (e.g., four streams for each operand) rather than the three streams of the present invention. As explained, machines do not have the capability for simultaneously providing 12 streams, so these machines were subject to inefficiencies during processing, since necessary data had to constantly be specifically retrieved from memory as new stream data was needed for the numerous streams.

A reduced number of streams (e.g., one stream per operand, for a total of only three streams in a level 3 processing involving three operands) is possible in the claimed invention because of the use of the register block format, wherein the blocks of data presented stride one to the processor unit have been predetermined to be arranged as needed for the matrix processing. The register block format was not known at the time of the cited prior art reference.

Thus, the register block format provides the capability of converting matrix data conventionally stored in standard format (e.g., column major or row major, depending upon the computer language being used) into a non-standard format wherein the matrix data has been specifically rearranged for the intended processing. Therefore, in the claimed invention, the register block format provides the mechanism to present a single stream of matrix data, respectively, for each of the three operands involved. Again, this capability was not available for the technique described in the cited reference.

Moreover, the register block format can be further refined to provide stride one data movement, meaning that the data within these blocks are contiguous and the blocks are arranged in the order that they will be consumed during the processing and will be arranged in memory to honor the stride one format normally used for memory data retrieval, thereby overcoming some of the inefficiencies of conventional matrix storage using standard format.

Applicants indicated that they would attempt to provide claim language that would more precisely define the invention, as well as remove the words considered by the Examiner as being indefinite or lacking clear support. Applicants also agreed to cite paragraphs in the other co-pending applications for wording from these co-pending applications being imported by reference into the specification of the present application.

Dr. Gustavson also explained how the present invention relied upon the register block

format, as demonstrated, for example by the description at line 7 of page 17, and as more fully described in co-pending application, US Patent Application S/N 10/671,888, from which co-pending application various aspects and descriptions were incorporated into the present application by the previous amendment. Dr. Gustavson also indicated how various paragraphs of the current rejection (e.g., paragraphs 54 and 62) were resolved by clarifying the register block format in the context of the present invention. Finally, Dr. Gustavson again described how the prior art did not address SIMD machines (e.g., SIMD, $k > 1$).

Claims 1-9 and 11-16 are all the claims presently pending in the application. Claims 10 and 17-20 are canceled, including claims 17-19 as newly-canceled to attempt to expedite prosecution by preemptively precluding a rejection that these claims might be construed as directed to non-statutory subject matter.

It is noted that Applicants specifically state that no amendment to any claim herein, if any, should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to the specification revisions previously proposed. The above specification revisions are believed to accommodate the Examiner's concerns. Support for the underlined wording above, in the second paragraph of the specification revision, is found in paragraphs [0073-0074] of the third of the listed co-pending applications, published as US Patent Application Publication No. 2005/0071409.

Claims 1-9 and 11-19 stand rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the written description requirement, and under 35 U.S.C. § 112, second paragraph, as being indefinite. Applicants believe that the above claim amendments and specification revisions appropriately address the Examiner's concerns and respectfully request that the Examiner reconsider and withdraw these rejections.

It is noted that the final limitation of the independent claims, including independent claim 6, the subject of the rejection described in paragraph 9 on page 5 of the Office Action, is believed to be fully supported in the present application in the description of paragraph [0062] of the published document, US Patent Publication No. 2005/0071405, for the instant application. It is believed that this final limitation of claim 6 cannot be interpreted as consisting of a single stream, as suggested in this paragraph 9, since the limitation clearly describes "three data streams" in its initial clause.

Should the Examiner continue to have additional reservations about claim language,

Applicants request that the Examiner contact the undersigned Applicants' representative at the direct line contact listed.

Claims 1-9 and 11-19 stand rejected under 35 U.S.C. § 102(b) as anticipated by Gustavson et al., "Superscalar GEMM-based Level 3 BLAS – The On-going Evolution of a Portable and High-Performance Library." As explained during the above-mentioned telephone interview, this previous work by co-inventor Dr. Gustavson differed from the claimed invention in at least the following ways:

1. There were 12 (or more) streams of data in the technology of this prior art reference. This number of streams is inefficient, since machines of that era did not support this many streams. The present invention uses only three streams (e.g., one stream per operand), each stream being contiguous data for that operand.

2. This reduced number of streams of the present invention (i.e., 3 streams, one per each operand A,B,C) is due to the utilization of the register block format, described in the third of the identified co-pending applications, as preliminarily rearranging the data of each operand to be in small blocks (e.g., 2x2 blocks) that will be stored as contiguous data for that stream in the order necessary for the processing. The 2x2 block is a "pseudo-matrix" described in the 3rd co-pending application that was presented as an exemplary demonstration of the register block format. As per discussion during the above-referenced telephone interview, the specification of the present application has been amended to incorporate additional discussion on the register block format, as requested by the Examiner.

3. The machines used in the cited reference by Dr. Gustavson did not SIMD ($k > 1$) capability. The 2x2 blocks of the pseudo-matrix example of the third co-pending application was an example of newer machines having a "quad load" capability for the instruction to load data from cache into the FPU, meaning that $k = 4$ for that instruction.

Applicants believe that the above specification and claim amendments adequately distinguish the claimed invention from this prior art reference, in view of the distinctions listed above and discussed during the above-referenced telephone interview.

Accordingly, Applicants believe that this rejection is rendered moot by the above claim amendments and respectfully request that the Examiner reconsider and withdraw this rejection.

FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 1-9 and 11-16, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

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